Software Reconfigurable Processor Technologies: The Key to Long-Life Infrastructure for Future Space Missions

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Abstract

We present an overview of long-life reconfigurable processor technologies and of a specific architecture for implementing a *software reconfigurable* (*software-defined*) *network processor* for space applications. A prototype of the software defined reconfigurable processor described here is currently operating in the laboratory at the Jet Propulsion Laboratory. The reconfigurable processor performs the functions of the physical layer (software radio), namely modulation, demodulation, pulse-shaping, error correction coding and decoding, as well as the data link layer, network layer, transport layer, and application layer science processing. The primary motivations behind the space-based software reconfiguarable network processor are the following:

- To enable rapid-prototyping and rapid space-qualified implementations of communications, navigation, and science signal processing functions.
- Providing long-life communications infrastructure enabled by on-orbit processor reconfiguration.
- Providing greatly improved science instrumentation and processing capabilities through on-orbit *science-driven reconfiguration.*

This work extends numerous advances in commercial industry as well as military software radio developments [1-5] to space-based radios and network processing. Such radios are software-defined while the implementation of the radio and other network functions are generally performed in combinations of the following software-defined processors: generic software processors, field programmable gate arrays (FPGAs), digital signal processors (DSPs), as well as tradition digital and mixed-signal applications specific integrated circuits (ASICs) and discrete analog-circuits. The development of such radios requires, and the network processor presented here, requires defining the correct combination of the processing methods outlined above.

Introduction

Many of the motivations for a space-based reconfigurable processor are similar to those driving reconfigurable processor efforts in private industry, in particular the cell-phone industry. Like cellular phones space-based processors need long-life and during this lifetime diverse applications arise. These potential applications cannot be anticipated at product/mission launch and the value of adapting to these unpredictable needs is extremely high, driving the need for reconfigurability [1].

The reconfigurable processor architecture, a composite of the processors listed previously, is determined by making trades between complexity, cost, development time, mass and size, flexibility, power consumption, and reliability to achieve system requirements. Given the variety of processors available in the commercial sector and the varying development platforms, these trades are extraordinarily complex.

We present high-level design paradigms and a generic reconfigurable processor architecture for providing tremendous flexibility, which in this instance leads to long-life, concurrent mission reconfigurability, and rapid prototyping of a wide variety of signal processing functions.

The high-level description of the functions of the space-based reconfigurable network processor is that it serves as communications infrastructure, science instrument and science data processor, and navigation infrastructure. Figure 1 is a conceptual illustration of these functions and how they are implemented. The network processor is represented in conventional network layers (layers 1, 2, 3, 4, and 7 of the OSI network model).

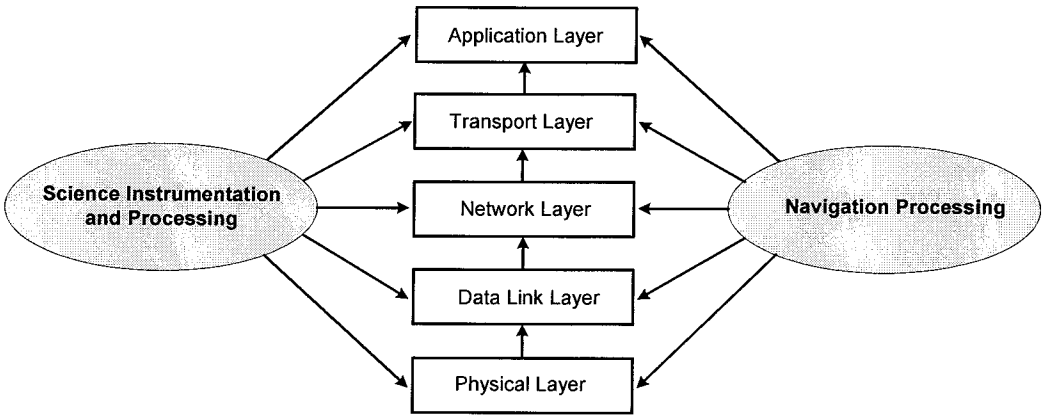

Figure 1. Model of Science, Navigation, and Communications Processing

Figure 2 illustrates a conceptual picture of the network layers implemented across a reconfigurable processor. This example assumes a Xilinx 1 million gate FPGA and a 700 Mhz Power PC processor. Note that the configuration of the software and hardware processors is defined by software control.

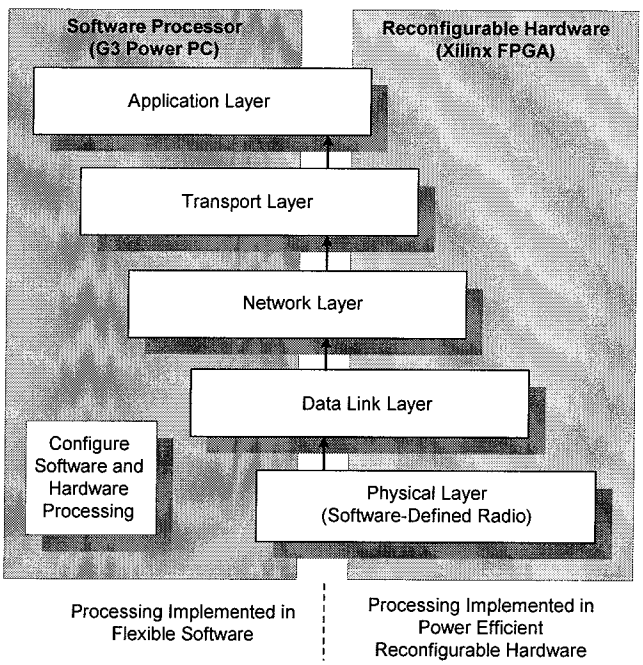

Figure 2. Network Layers Implemented in a Reconfigurable Processor

Figure 3 illustrates a new possible paradigm for communications, navigation, and science requirements, developed by scientist and mission planners, to be integrated into the

network processor during an operational mission. Note that with reconfigurable processor technology science processing may be modified by mission planners as a result of the science data acquired during a mission.

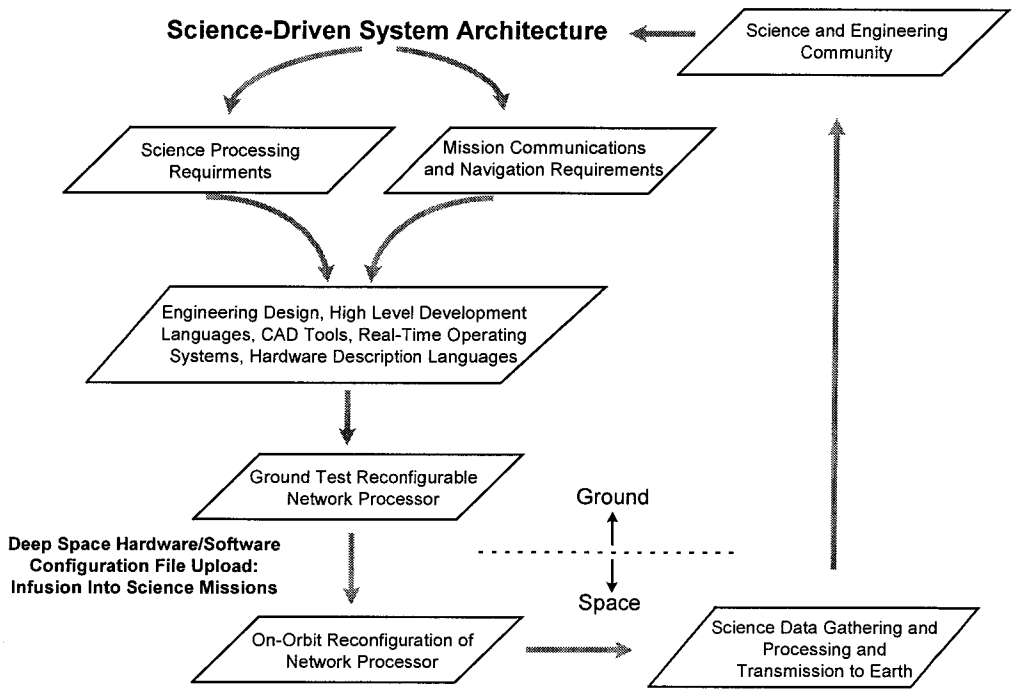

Figure 3. On-Orbit Reconfiguration of Network Processor

Example: Physical Layer Software Radio

The deep space communications channel has very unique problems as compared to terrestrial communications. Primarily the channel distances involved are often many orders of magnitude larger than those of terrestrial communications. This makes power efficient transmission of information very critical. Power efficiency may be increased through the use of error control coding. Turbo-codes and low-density parity check codes offer performance very close to the Shannon limit, the minimum bit-error rate possible for a given signal-to-noise ratio. The advantages these modern error control codes exhibit over more conventional codes are well known and are on the order of many dB in required transmit power savings. Unfortunately the optimal decoders for many such codes are very computationally intensive, making them prohibitively complicated to implement for high data rates. There is little doubt in the academic community that decoders for these codes will be developed with significantly less complex implementations. In other words, although it would be a significant undertaking to implement a turbo decoder for data rates in excess of a few Mbps in today's space qualified processing technology, in a few years it is very probable that simplified decoders will be developed to be readily implemented in this processing technology. Implementing such decoders in a processor years after launch is possible with the paradigm illustrated in Figure 3.

Example: Navigation and Ranging

The processor may be used to perform navigation functions. In some cases the physical layer radio processing may need to be reconfigured to perform ranging. Using the paradigm of Figure 3 the modulation type processed by the physical layer and

navigation algorithms processed by the application layer may be reconfigured from the ground.

Example: Science Instrument Processing

The argument for the need for on-orbit science processing enhancements is also extremely compelling. The science goals and therefore the exact processing desired may change after mission launch. An example of this was the desire to change the way occultation measurements were made in the *CHAMP* mission after launch. *Mars Scout* atmospheric occultation measurements may also reveal that changes should be made in the way these measurements are made.

The concept of the reconfigurable processor as a science-defined processor may be extended to include time-varying science processing. Due to the reconfigurable nature of the network processor it may fill the role of a large number of temporally separated science instrument processors.

Laboratory Prototype

A prototype of the reconfigurable processor illustrated in Figure 2 is currently operating in the laboratory. To date the physical, data link, and transport layers have been implemented and demonstrated. The physical layer consists of a reconfigurable BPSK demodulator, the data link layer consists of an implementation of the majority of the Proximity-1 protocol draft recommendation by the Consultative Committee for Space Data Systems (CCSDS), and the transport layer consists of a commercial transport layer protocol. The processor has been demonstrated in a two-way communications link with data rates as high as 1 Mbps per channel.

Conclusion

We have provided a brief overview of software reconfigurable processor technologies and the paradigms used in development of the prototype software reconfigurable network processor operating in the laboratory at JPL. The authors believe reconfigurable processor technology leads directly to a tremendous increase in the diversity of applications of signal processing for science benefits as compared to traditional processor technologies, and can provide long-life infrastructure support. Mission concurrent reconfiguration enables multi-mission support, reconfigurable communications and navigation infrastructure, and science instrumentation and processing improvements. Examples of missions planning to use the reconfigurable architecture of Figure 2 and variations developed at JPL include Space Technology 5 (ST-5) in '03, the Starlight instrument for AFF in '06, and the Neige experiments on Mars Premier orbiter in '05. The reconfigurable processor may also be appropriate for Mars Scout missions in '07 as well as future Mars Network payloads.

References

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